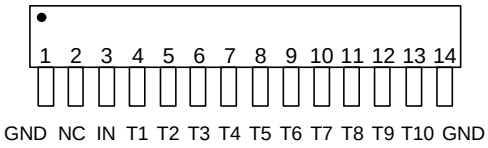
10-TAP SIP DELAY LINE
$T_D/T_R = 5$
(SERIES 1507)

data delay devices, inc.

FEATURES

- 10 taps of equal delay increment
- Very narrow device (SIP package)
- Stackable for PC board economy
- Low profile
- Epoxy encapsulated
- Meets or exceeds MIL-D-23859C

PACKAGES



1507-xxz
xx = Delay (T_D)
z = Impedance Code

FUNCTIONAL DESCRIPTION

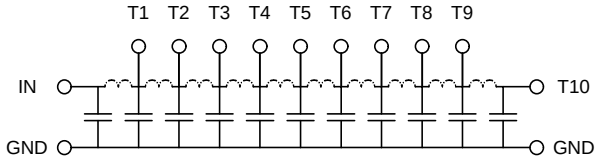
The 1507-series device is a fixed, single-input, ten-output, passive delay line. The signal input (IN) is reproduced at the outputs (T1-T10) in equal increments. The delay from IN to T10 (T_D) is given by the device dash number. The characteristic impedance of the line is given by the letter code that follows the dash number (See Table). The rise time (T_R) of the line is 10% of T_D, and the 3dB bandwidth is given by 3.5 / T_D.

PIN DESCRIPTIONS

IN	Signal Input
T1-T10	Tap Outputs
GND	Ground

SERIES SPECIFICATIONS

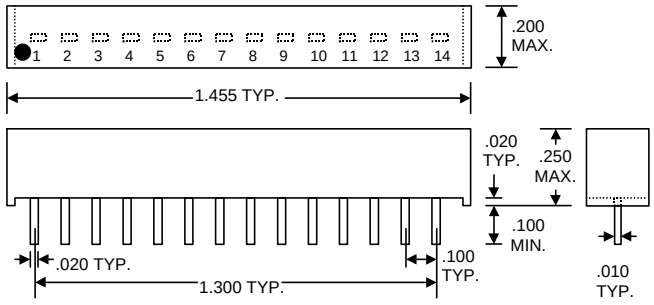
- **Dielectric breakdown:** 50 Vdc
- **Distortion @ output:** 10% max.
- **Operating temperature:** -55°C to +125°C
- **Storage temperature:** -55°C to +125°C
- **Temperature coefficient:** 100 PPM/°C



Functional Diagram

DASH NUMBER SPECIFICATIONS

Part Number	T_D (ns)	Delay per Tap (ns)	T_R (ns)	Impedance (Ω)	R_{DC} (Ω)
1507-20A	20.0 ± 2.0	2.0 ± 0.4	4.0	50	1.0
1507-40A	40.0 ± 2.0	4.0 ± 1.0	8.0	50	1.5
1507-50A	50.0 ± 2.5	5.0 ± 1.5	9.0	50	1.5
1507-100A	100 ± 5.0	10.0 ± 2.0	18.0	50	2.0
1507-150A	150 ± 7.5	15.0 ± 2.0	28.0	50	3.0
1507-200A	200 ± 10.0	20.0 ± 3.0	38.0	50	4.0
1507-20B	20.0 ± 2.0	2.0 ± 0.4	4.0	100	1.5
1507-50B	50.0 ± 2.5	5.0 ± 1.5	9.0	100	2.0
1507-100B	100 ± 5.0	10.0 ± 2.0	18.0	100	4.0
1507-200B	200 ± 10.0	20.0 ± 3.0	38.0	100	6.0
1507-250B	250 ± 13.0	25.0 ± 4.0	48.0	100	7.0
1507-20C	20.0 ± 2.0	2.0 ± 0.4	4.0	200	3.0
1507-50C	50.0 ± 2.5	5.0 ± 1.5	9.0	200	4.5
1507-100C	100 ± 5.0	10.0 ± 2.0	18.0	200	6.0
1507-200C	200 ± 13.0	20.0 ± 3.0	38.0	200	9.0
1507-50G	50.0 ± 2.5	5.0 ± 1.5	9.0	500	6.0
1507-100G	100 ± 5.0	10.0 ± 2.0	18.0	500	10.0
1507-200G	200 ± 10.0	20.0 ± 3.0	38.0	500	30.0
1507-300G	300 ± 15.0	30.0 ± 4.0	58.0	500	30.0
1507-500G	500 ± 25.0	50.0 ± 5.0	98.0	500	55.0



Package Dimensions

PASSIVE DELAY LINE TEST SPECIFICATIONS

TEST CONDITIONS

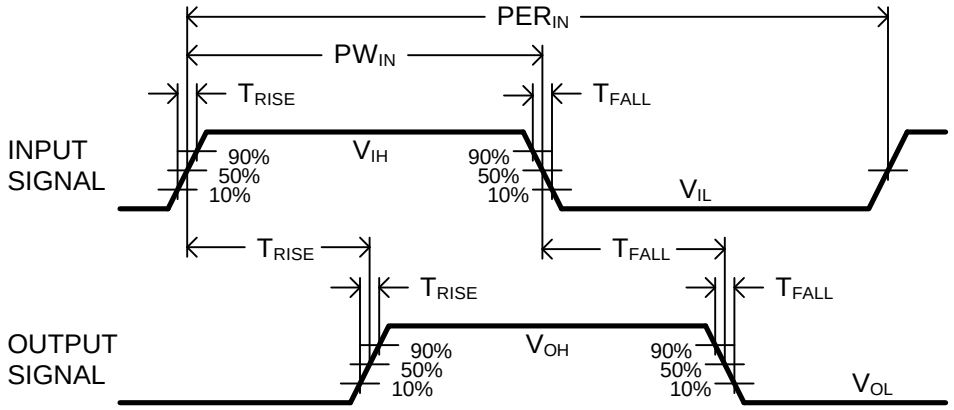
INPUT:

Ambient Temperature:	25°C ± 3°C
Input Pulse:	High = 3.0V typical Low = 0.0V typical
Source Impedance:	50Ω Max.
Rise/Fall Time:	3.0 ns Max. (measured at 10% and 90% levels)
Pulse Width (T_D <= 75ns):	PW_{IN} = 100ns
Period (T_D <= 75ns):	PER_{IN} = 1000ns
Pulse Width (T_D > 75ns):	PW_{IN} = 2 x T_D
Period (T_D > 75ns):	PER_{IN} = 10 x T_D

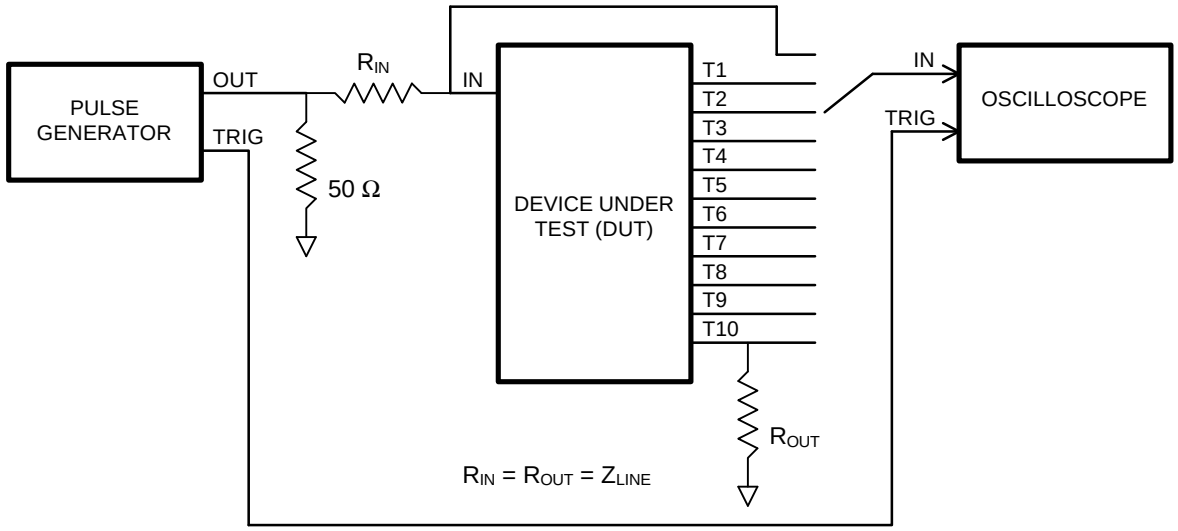
OUTPUT:

R_{load}:	10MΩ
C_{load}:	10pf
Threshold:	50% (Rising & Falling)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Timing Diagram For Testing



Test Setup